

## CLAIMS

What is claimed is:

1) A system for reducing power in memory cells comprising:

- 2 a) a circuit, the circuit having an input and an output;
- b) wherein the input is connected to a wordline of the memory cells;
- 4 c) wherein the output is connected to a positive voltage supply node of the memory cells;
- 6 d) wherein a first voltage applied to the output is reduced by at least one  $V_t$  from a supply voltage, VDD, when the wordline is inactive;
- 8 e) wherein a second voltage applied to the output is near the supply voltage, VDD, when the wordline is active.

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2) The system as in Claim 1 wherein the memory cells are SRAM cells.

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3) The system as in Claim 1 wherein the memory cells are DRAM cells.

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4) The system as in Claim 1 wherein the circuit comprises:

- 2 a) an inverter, the inverter having an input and an output;
- b) an NFET, the NFET having a gate, a drain, and a source;
- 4 c) a PFET, the PFET having a gate, a drain, and a source;
- d) wherein the input of the inverter is connected to the input of the circuit;
- 6 e) wherein the output of the inverter is connected to the gate of the PFET;

- 8 f) wherein the source of the PFET, the gate of the NFET, and drain of the NFET are connected to the supply voltage, VDD;
- 10 g) wherein the drain of the PFET and the source of the NFET are connected to the output of the circuit.

5) A system as in Claim 1 wherein the circuit comprises:

- 2 a) a first NFET, the first NFET having a gate, a drain, and a source;
- b) a second NFET, the second NFET having a gate, a drain, and a source;
- 4 c) a third NFET, the third NFET having a gate, a drain, and a source;
- d) a fourth NFET, the fourth NFET having a gate, a drain, and a source;
- 6 e) wherein the gate of the first NFET is connected to the input of the circuit;
- f) wherein the drain and the source of the first NFET is connected to the
- 8 source of the second NFET and to the gate of the third NFET;
- g) wherein the drain of the second NFET, the gate of the second NFET, the
- 10 drain of the third NFET, the drain of the fourth NFET, and the gate of the fourth NFET are connected to the supply voltage, VDD;
- 12 h) wherein the source of the third NFET, and the source of the fourth NFET are connected to the output of circuit.

6) A system for reducing power in memory cells comprising:

- 2 a) a circuit, the circuit having an input, a first output, and a second output;
- b) wherein the input is connected to an active-low wordline;
- 4 c) wherein the first output is connected to a local wordline of the memory cells;

- 6 d) wherein the second output is connected to a positive voltage supply node  
of the memory cells;
- 8 e) wherein a first voltage applied to the second output is reduced by at least  
one  $V_t$  from a supply voltage, VDD, when the active-low wordline is high;
- 10 f) wherein a second voltage applied to the second output is near the supply  
voltage, VDD, when the active-low wordline is low.

12 7) The system as in Claim 6 wherein the circuit comprises:

- 2 a) an inverter, the inverter having an input and an output;
- b) an NFET, the NFET having a gate, a drain, and a source;
- 4 c) a PFET, the PFET having a gate, a drain, and a source;
- d) wherein the input of the inverter is connected to the input of the circuit;
- 6 e) wherein the output of the inverter is connected to the first output of the  
circuit;
- 8 f) wherein the source of the PFET, the gate of the NFET, and drain of the  
NFET are connected to the supply voltage, VDD;
- 10 g) wherein drain of the PFET and the source of the NFET are connected to  
the second output of the circuit.

12 8) A method for manufacturing a circuit for reducing power in memory cells

2 comprising:

- a) fabricating an inverter, the inverter having an input and an output;
- 4 b) fabricating an NFET, the NFET having a gate, a drain, and a source;
- c) fabricating a PFET, the PFET having a gate, a drain, and a source;

- 6 d) wherein the input of the inverter is connected to a wordline of the memory  
cells;
- 8 e) wherein the output of the inverter is connected to the gate of the PFET;
- 10 f) wherein the source of the PFET, the gate of the NFET, and drain of the  
NFET are connected to the supply voltage, VDD;
- 12 g) where in drain of the PFET and the source of the NFET are connected to a  
positive voltage supply node of the memory cells.

14 9) A method for manufacturing a circuit for reducing power in memory cells

2 comprising:

- 4 a) fabricating a first NFET, the first NFET having a gate, a drain, and a  
source;
- 6 b) fabricating a second NFET, the second NFET having a gate, a drain, and a  
source;
- 8 c) fabricating a third NFET, the third NFET having a gate, a drain, and a  
source;
- 10 d) fabricating a fourth NFET, the fourth NFET having a gate, a drain, and a  
source;
- 12 e) wherein the gate of the first NFET is connected to the wordline of the  
memory cells;
- 14 f) wherein the drain and the source of the first NFET is connected to the  
source of the second NFET and to the gate of the third NFET;

g) wherein the drain of the second NFET, the gate of the second NFET, the  
drain of the third NFET, the drain of the fourth NFET, and the gate of the  
fourth NFET are connected to the supply voltage, VDD;

h) wherein the source of the third NFET, and the source of the fourth NFET  
are connected to a positive voltage supply node of the memory cells.

10) A method for manufacturing a circuit for reducing power in memory cells  
comprising:

a) fabricating an inverter, the inverter having an input and an output;

b) fabricating an NFET, the NFET having a gate, a drain, and a source;

c) fabricating a PFET, the PFET having a gate, a drain, and a source;

d) wherein the input of the inverter is connected to an active low  
wordline;

e) wherein the output of the inverter is connected to a local wordline of  
the memory cells;

f) wherein the source of the PFET, the gate of the NFET, and drain of the  
NFET are connected to the supply voltage, VDD;

g) wherein drain of the PFET and the source of the NFET are connected  
to a positive voltage supply node of the memory cells.